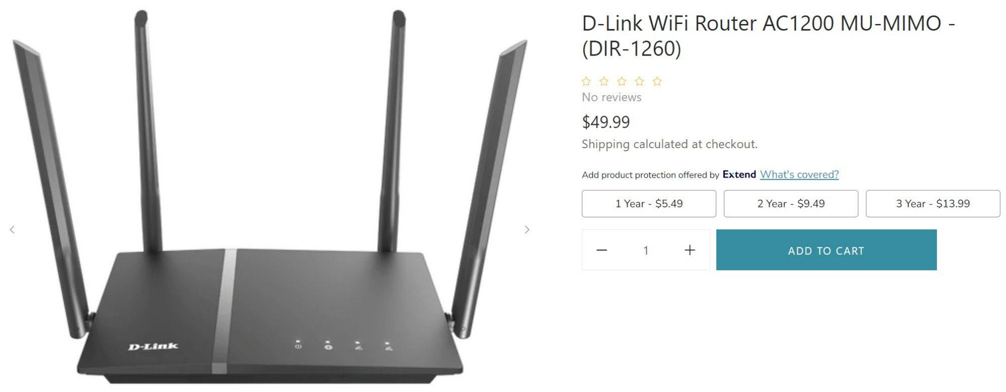
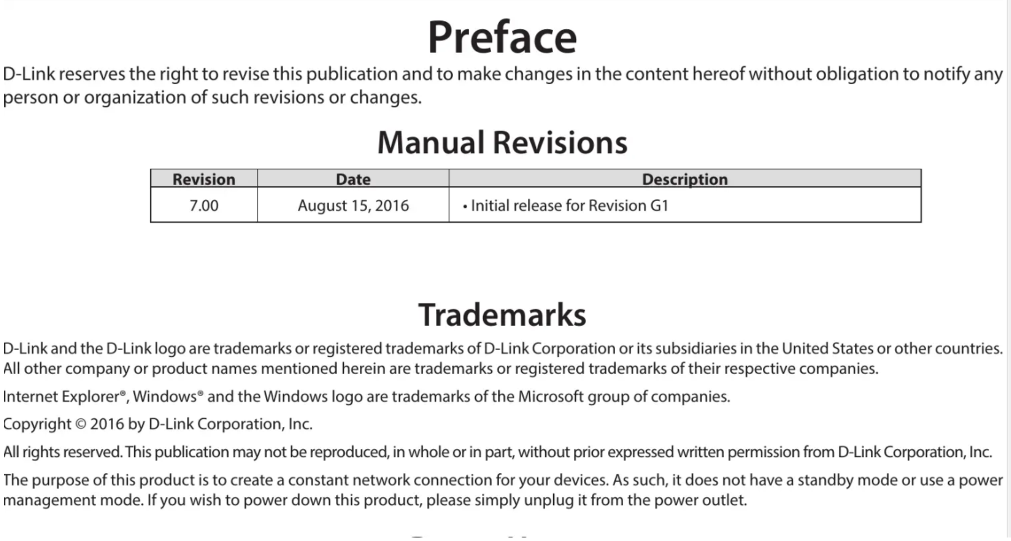
EXHIBIT 5

Exhibit 5: U.S. Patent No. 8,583,980

Claim 17	Identification
17[pre] A method of operating a transceiver, comprising:	To the extent the preamble is limiting, D-Link-branded devices, such as the D-Link WiFi Router AC1200 MU-MIMO, implement a method of operating a transceiver comprising the steps below.  D-Link WiFi Router AC1200 MU-MIMO - (DIR-1260) ☆☆☆☆☆ No reviews $49.99 Shipping calculated at checkout. Add product protection offered by **Extend** What's covered? https://shop.us.dlink.com/products/d-link-wifi-router-ac1200-mu-mimo

<table>
<tr><th>Claim 17</th><th>Identification</th></tr>
<tr><td></td><td>

User Manual
AC1200 Wi-Fi Gigabit Router

<h2>Preface</h2>
D-Link reserves the right to revise this publication and to make changes in the content hereof without obligation to notify any person or organization of such revisions or changes.
<h3>Manual Revisions</h3>
<table>
<tr><th>Revision</th><th>Date</th><th>Description</th></tr>
<tr><td>7.00</td><td>August 15, 2016</td><td>• Initial release for Revision G1</td></tr>
</table>
<h3>Trademarks</h3>
D-Link and the D-Link logo are trademarks or registered trademarks of D-Link Corporation or its subsidiaries in the United States or other countries. All other company or product names mentioned herein are trademarks or registered trademarks of their respective companies.
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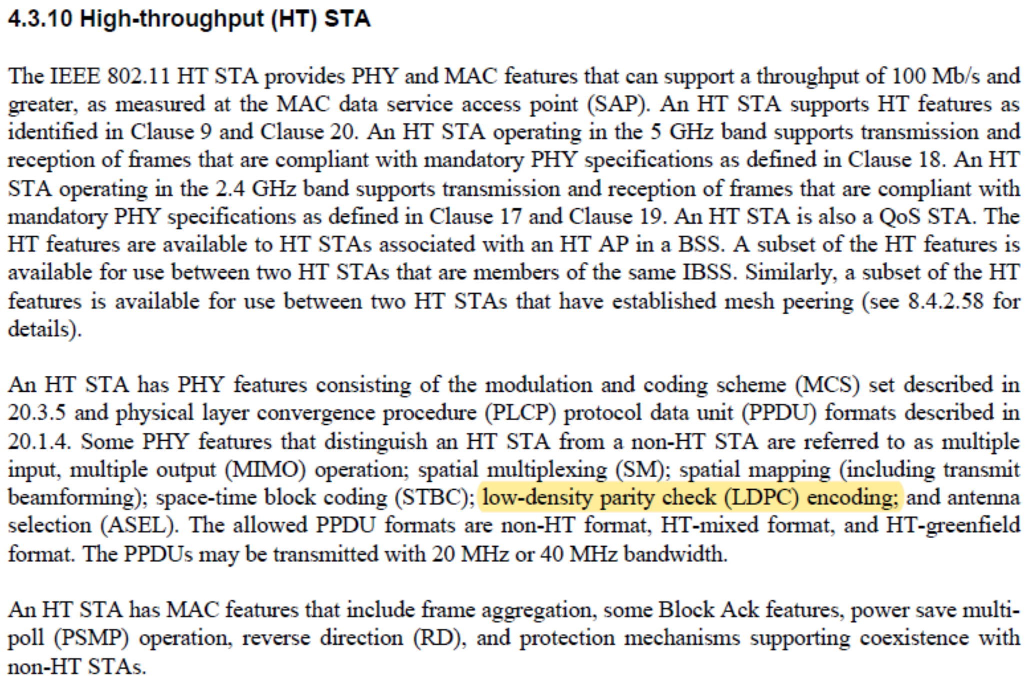
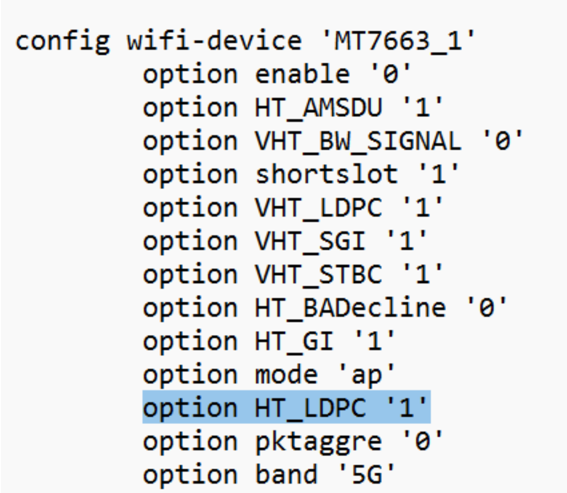
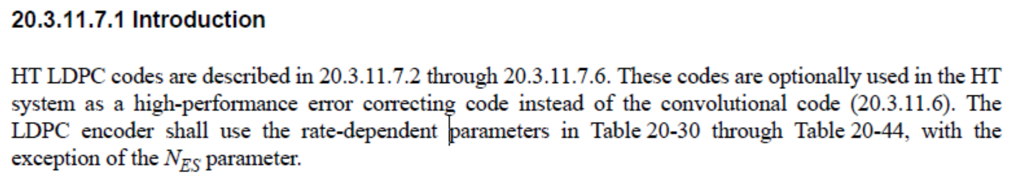
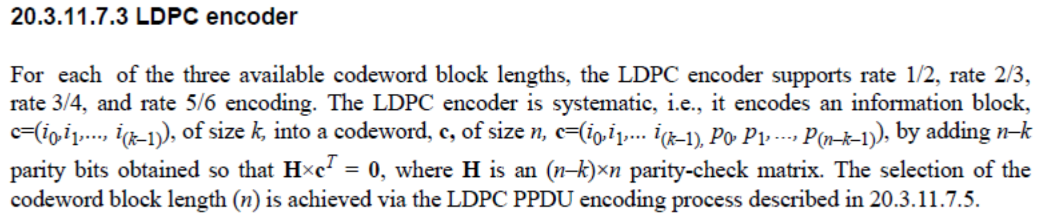
Copyright © 2016 by D-Link Corporation, Inc.
All rights reserved. This publication may not be reproduced, in whole or in part, without prior expressed written permission from D-Link Corporation, Inc.
The purpose of this product is to create a constant network connection for your devices. As such, it does not have a standby mode or use a power management mode. If you wish to power down this product, please simply unplug it from the power outlet.
</td></tr>
</table>

Claim 17	Identification
	 **4.3.10 High-throughput (HT) STA** The IEEE 802.11 HT STA provides PHY and MAC features that can support a throughput of 100 Mb/s and greater, as measured at the MAC data service access point (SAP). An HT STA supports HT features as identified in Clause 9 and Clause 20. An HT STA operating in the 5 GHz band supports transmission and reception of frames that are compliant with mandatory PHY specifications as defined in Clause 18. An HT STA operating in the 2.4 GHz band supports transmission and reception of frames that are compliant with mandatory PHY specifications as defined in Clause 17 and Clause 19. An HT STA is also a QoS STA. The HT features are available to HT STAs associated with an HT AP in a BSS. A subset of the HT features is available for use between two HT STAs that are members of the same IBSS. Similarly, a subset of the HT features is available for use between two HT STAs that have established mesh peering (see 8.4.2.58 for details). An HT STA has PHY features consisting of the modulation and coding scheme (MCS) set described in 20.3.5 and physical layer convergence procedure (PLCP) protocol data unit (PPDU) formats described in 20.1.4. Some PHY features that distinguish an HT STA from a non-HT STA are referred to as multiple input, multiple output (MIMO) operation; spatial multiplexing (SM); spatial mapping (including transmit beamforming); space-time block coding (STBC); low-density parity check (LDPC) encoding; and antenna selection (ASEL). The allowed PPDU formats are non-HT format, HT-mixed format, and HT-greenfield format. The PPDUs may be transmitted with 20 MHz or 40 MHz bandwidth. An HT STA has MAC features that include frame aggregation, some Block Ack features, power save multi-poll (PSMP) operation, reverse direction (RD), and protection mechanisms supporting coexistence with non-HT STAs. 802.11 (2012) LDPC is enabled for D-Link DIR-1260 with MT7663 chip.

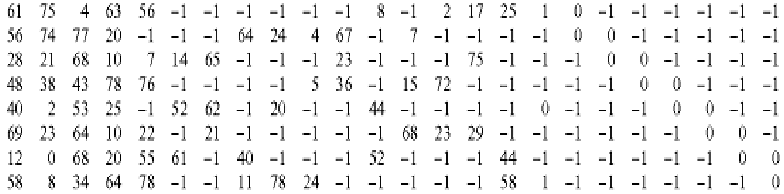
Claim 17	Identification
	

```
config wifi-device 'MT7663_1'
        option enable '0'
        option HT_AMSDU '1'
        option VHT_BW_SIGNAL '0'
        option shortslot '1'
        option VHT_LDPC '1'
        option VHT_SGI '1'
        option VHT_STBC '1'
        option HT_BADecline '0'
        option HT_GI '1'
        option mode 'ap'
        option HT_LDPC '1'
        option pktaggre '0'
        option band '5G'
```

	DIR1260_A1_V1.00B07_GPLCode_20201216.tar.gz\DIR1260_GPL_Release\vendors\DIR-1260\config\wireless_router
17[a] applying the following expanded parity check matrix to generate encoded data:	D-Link-branded devices (such the D-Link WiFi Router AC1200 MU-MIMO) apply the claimed expanded parity check matrix to generate encoded data:  **20.3.11.7.1 Introduction** HT LDPC codes are described in 20.3.11.7.2 through 20.3.11.7.6. These codes are optionally used in the HT system as a high-performance error correcting code instead of the convolutional code (20.3.11.6). The LDPC encoder shall use the rate-dependent parameters in Table 20-30 through Table 20-44, with the exception of the N_{ES} parameter. 802.11 (2012)

Claim 17	Identification
	 **20.3.11.7.3 LDPC encoder** For each of the three available codeword block lengths, the LDPC encoder supports rate 1/2, rate 2/3, rate 3/4, and rate 5/6 encoding. The LDPC encoder is systematic, i.e., it encodes an information block, $\mathbf{c}=(i_0,i_1,\ldots, i_{(k-1)})$, of size k, into a codeword, **c**, of size n, $\mathbf{c}=(i_0,i_1,\ldots i_{(k-1)}, p_0, p_1, \ldots, p_{(n-k-1)})$, by adding $n-k$ parity bits obtained so that $\mathbf{H}\times\mathbf{c}^T = \mathbf{0}$, where **H** is an $(n-k)\times n$ parity-check matrix. The selection of the codeword block length (n) is achieved via the LDPC PPDU encoding process described in 20.3.11.7.5. 802.11 (2012)

Claim 17



61	75	4	63	56	−1	−1	−1	−1	−1	−1	8	−1	2	17	25	1	0	−1	−1	−1	−1	−1	−1
56	74	77	20	−1	−1	−1	64	24	4	67	−1	7	−1	−1	−1	−1	0	0	−1	−1	−1	−1	−1
28	21	68	10	7	14	65	−1	−1	−1	23	−1	−1	−1	75	−1	−1	−1	0	0	−1	−1	−1	−1
48	38	43	78	76	−1	−1	−1	−1	5	36	−1	15	72	−1	−1	−1	−1	−1	0	0	−1	−1	−1
40	2	53	25	−1	52	62	−1	20	−1	−1	44	−1	−1	−1	−1	0	−1	−1	−1	0	0	−1	−1
69	23	64	10	22	−1	21	−1	−1	−1	−1	−1	68	23	29	−1	−1	−1	−1	−1	−1	0	0	−1
12	0	68	20	55	61	−1	40	−1	−1	−1	52	−1	−1	−1	44	−1	−1	−1	−1	−1	−1	0	0
58	8	34	64	78	−1	−1	11	78	24	−1	−1	−1	−1	−1	58	1	−1	−1	−1	−1	−1	−1	0

wherein −1 represents an 81×81 all-zero square matrix, and any other integer, Sij, represents an 81×81 identity matrix circularly right shifted by a shift amount equal to Sij;

Identification

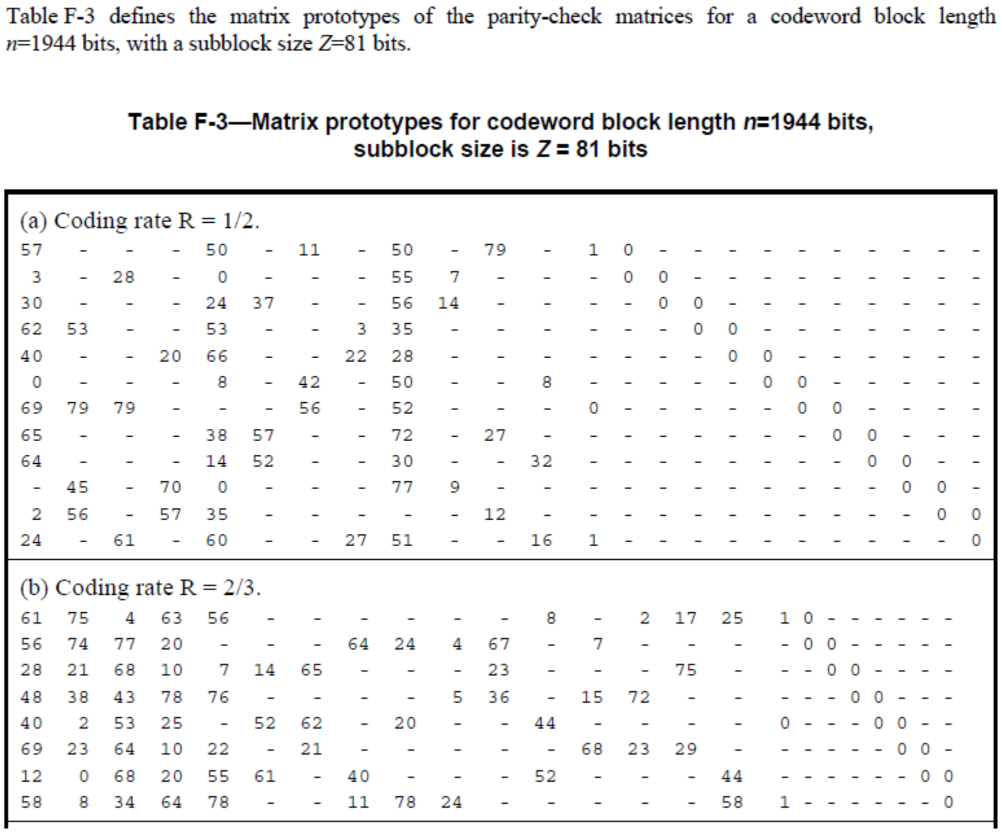


Table F-3 defines the matrix prototypes of the parity-check matrices for a codeword block length *n*=1944 bits, with a subblock size *Z*=81 bits.

Table F-3—Matrix prototypes for codeword block length *n*=1944 bits, subblock size is *Z* = 81 bits

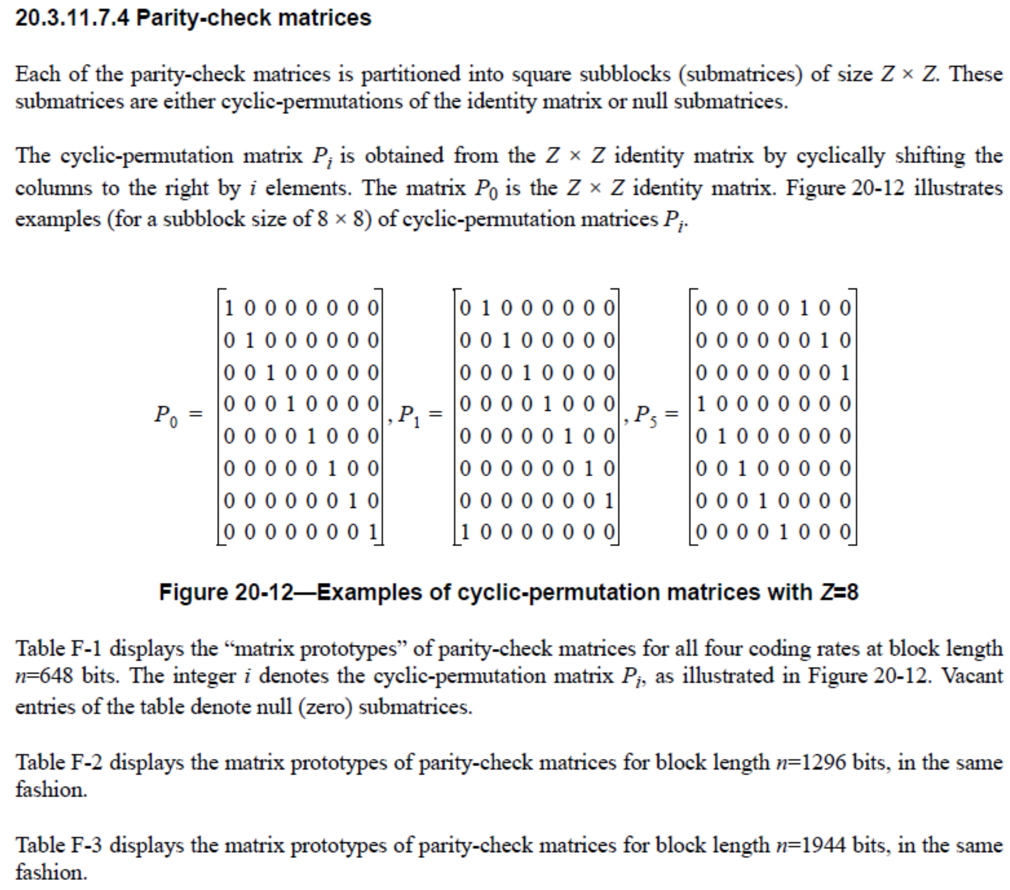
(a) Coding rate R = 1/2.

57	-	-	-	50	-	11	-	50	-	79	-	1	0	-	-	-	-	-	-	-	-	-	-
3	-	28	-	0	-	-	-	55	7	-	-	-	0	0	-	-	-	-	-	-	-	-	-
30	-	-	-	24	37	-	-	56	14	-	-	-	-	0	0	-	-	-	-	-	-	-	-
62	53	-	-	53	-	-	3	35	-	-	-	-	-	-	0	0	-	-	-	-	-	-	-
40	-	-	20	66	-	-	22	28	-	-	-	-	-	-	-	0	0	-	-	-	-	-	-
0	-	-	-	8	-	42	-	50	-	-	8	-	-	-	-	-	0	0	-	-	-	-	-
69	79	79	-	-	-	56	-	52	-	-	-	0	-	-	-	-	-	0	0	-	-	-	-
65	-	-	-	38	57	-	-	72	-	27	-	-	-	-	-	-	-	-	0	0	-	-	-
64	-	-	-	14	52	-	-	30	-	-	32	-	-	-	-	-	-	-	-	0	0	-	-
-	45	-	70	0	-	-	-	77	9	-	-	-	-	-	-	-	-	-	-	-	0	0	-
2	56	-	57	35	-	-	-	-	-	12	-	-	-	-	-	-	-	-	-	-	-	0	0
24	-	61	-	60	-	-	27	51	-	-	16	1	-	-	-	-	-	-	-	-	-	-	0

(b) Coding rate R = 2/3.

61	75	4	63	56	-	-	-	-	-	-	8	-	2	17	25	1	0	-	-	-	-	-	-
56	74	77	20	-	-	-	64	24	4	67	-	7	-	-	-	-	0	0	-	-	-	-	-
28	21	68	10	7	14	65	-	-	-	23	-	-	-	75	-	-	-	0	0	-	-	-	-
48	38	43	78	76	-	-	-	-	5	36	-	15	72	-	-	-	-	-	0	0	-	-	-
40	2	53	25	-	52	62	-	20	-	-	44	-	-	-	-	0	-	-	-	0	0	-	-
69	23	64	10	22	-	21	-	-	-	-	-	68	23	29	-	-	-	-	-	-	0	0	-
12	0	68	20	55	61	-	40	-	-	-	52	-	-	-	44	-	-	-	-	-	-	0	0
58	8	34	64	78	-	-	11	78	24	-	-	-	-	-	58	1	-	-	-	-	-	-	0

802.11 (2012)

Claim 17	Identification
	 **20.3.11.7.4 Parity-check matrices** Each of the parity-check matrices is partitioned into square subblocks (submatrices) of size $Z \times Z$. These submatrices are either cyclic-permutations of the identity matrix or null submatrices. The cyclic-permutation matrix P_i is obtained from the $Z \times Z$ identity matrix by cyclically shifting the columns to the right by i elements. The matrix P_0 is the $Z \times Z$ identity matrix. Figure 20-12 illustrates examples (for a subblock size of 8 × 8) of cyclic-permutation matrices P_i. $$P_0 = \begin{bmatrix} 1&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \end{bmatrix}, P_1 = \begin{bmatrix} 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \\ 1&0&0&0&0&0&0&0 \end{bmatrix}, P_5 = \begin{bmatrix} 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \\ 1&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \end{bmatrix}$$ **Figure 20-12—Examples of cyclic-permutation matrices with Z=8** Table F-1 displays the “matrix prototypes” of parity-check matrices for all four coding rates at block length n=648 bits. The integer i denotes the cyclic-permutation matrix P_i, as illustrated in Figure 20-12. Vacant entries of the table denote null (zero) submatrices. Table F-2 displays the matrix prototypes of parity-check matrices for block length n=1296 bits, in the same fashion. Table F-3 displays the matrix prototypes of parity-check matrices for block length n=1944 bits, in the same fashion. 802.11 (2012)
and applying the expanded parity check matrix to generate decoded data.	D-Link-branded devices (such the D-Link WiFi Router AC1200 MU-MIMO) apply the claimed expanded parity check matrix to generate decoded data:

Claim 17	Identification

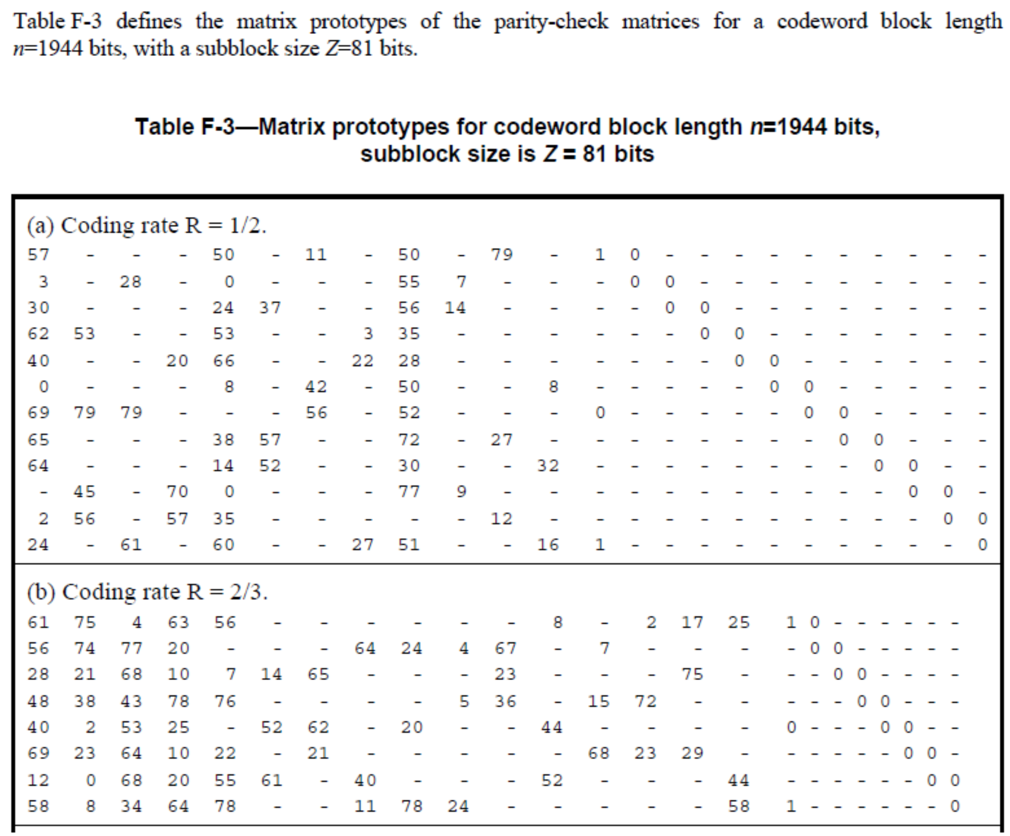


Table F-3 defines the matrix prototypes of the parity-check matrices for a codeword block length *n*=1944 bits, with a subblock size *Z*=81 bits.

Table F-3—Matrix prototypes for codeword block length *n*=1944 bits, subblock size is *Z* = 81 bits

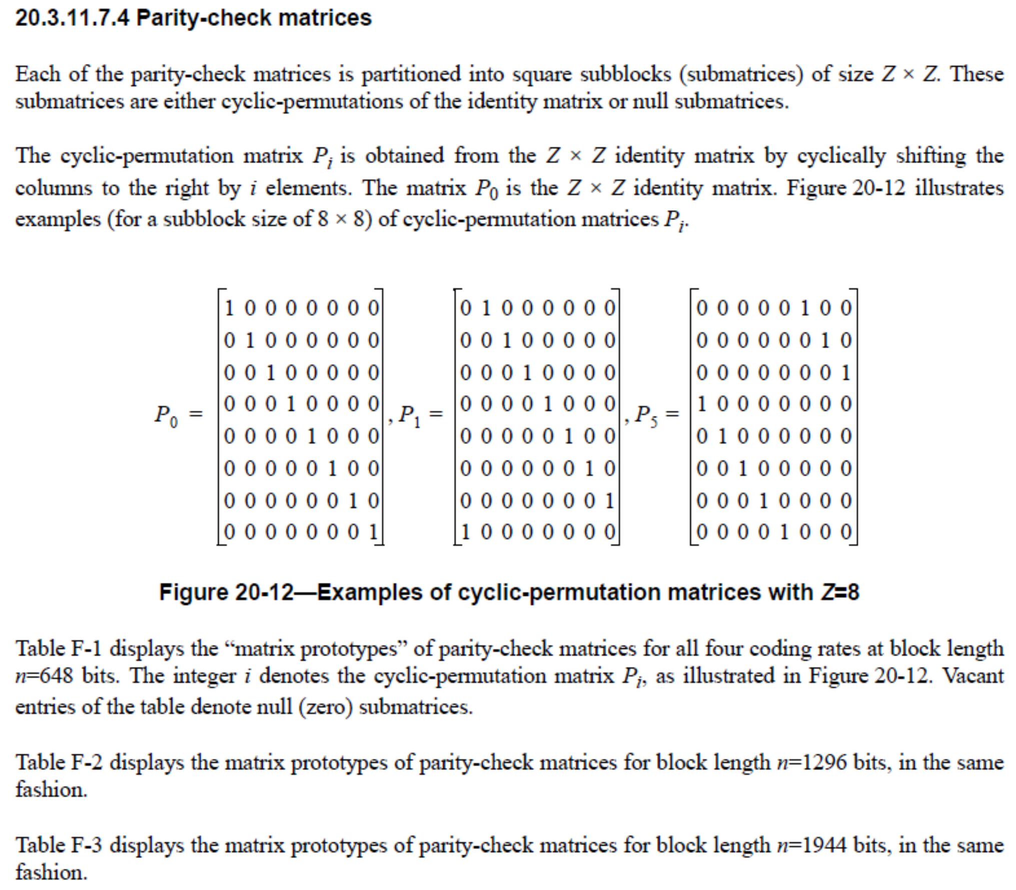
(a) Coding rate R = 1/2.

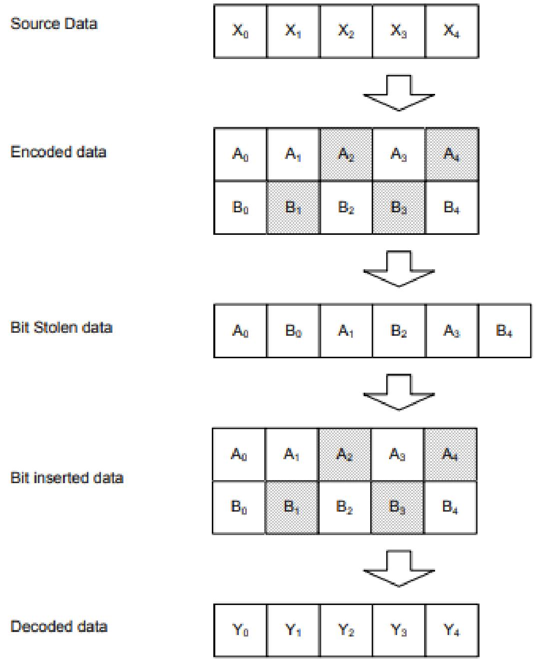
57	-	-	-	50	-	11	-	50	-	79	-	1	0	-	-	-	-	-	-	-	-	-	-
3	-	28	-	0	-	-	-	55	7	-	-	-	0	0	-	-	-	-	-	-	-	-	-
30	-	-	-	24	37	-	-	56	14	-	-	-	-	0	0	-	-	-	-	-	-	-	-
62	53	-	-	53	-	-	3	35	-	-	-	-	-	-	0	0	-	-	-	-	-	-	-
40	-	-	20	66	-	-	22	28	-	-	-	-	-	-	-	0	0	-	-	-	-	-	-
0	-	-	-	8	-	42	-	50	-	-	8	-	-	-	-	-	0	0	-	-	-	-	-
69	79	79	-	-	-	56	-	52	-	-	-	0	-	-	-	-	-	0	0	-	-	-	-
65	-	-	-	38	57	-	-	72	-	27	-	-	-	-	-	-	-	-	0	0	-	-	-
64	-	-	-	14	52	-	-	30	-	-	32	-	-	-	-	-	-	-	-	0	0	-	-
-	45	-	70	0	-	-	-	77	9	-	-	-	-	-	-	-	-	-	-	-	0	0	-
2	56	-	57	35	-	-	-	-	-	12	-	-	-	-	-	-	-	-	-	-	-	0	0
24	-	61	-	60	-	-	27	51	-	-	16	1	-	-	-	-	-	-	-	-	-	-	0

(b) Coding rate R = 2/3.

61	75	4	63	56	-	-	-	-	-	-	8	-	2	17	25	1	0	-	-	-	-	-	-
56	74	77	20	-	-	-	64	24	4	67	-	7	-	-	-	-	0	0	-	-	-	-	-
28	21	68	10	7	14	65	-	-	-	23	-	-	-	75	-	-	-	0	0	-	-	-	-
48	38	43	78	76	-	-	-	-	5	36	-	15	72	-	-	-	-	-	0	0	-	-	-
40	2	53	25	-	52	62	-	20	-	-	44	-	-	-	-	0	-	-	-	0	0	-	-
69	23	64	10	22	-	21	-	-	-	-	-	68	23	29	-	-	-	-	-	-	0	0	-
12	0	68	20	55	61	-	40	-	-	-	52	-	-	-	44	-	-	-	-	-	-	0	0
58	8	34	64	78	-	-	11	78	24	-	-	-	-	-	58	1	-	-	-	-	-	-	0

802.11 (2012)

Claim 17	Identification
	 **20.3.11.7.4 Parity-check matrices** Each of the parity-check matrices is partitioned into square subblocks (submatrices) of size $Z \times Z$. These submatrices are either cyclic-permutations of the identity matrix or null submatrices. The cyclic-permutation matrix P_i is obtained from the $Z \times Z$ identity matrix by cyclically shifting the columns to the right by i elements. The matrix P_0 is the $Z \times Z$ identity matrix. Figure 20-12 illustrates examples (for a subblock size of 8 × 8) of cyclic-permutation matrices P_i. $P_0 = \begin{bmatrix} 1&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \end{bmatrix}, P_1 = \begin{bmatrix} 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \\ 1&0&0&0&0&0&0&0 \end{bmatrix}, P_5 = \begin{bmatrix} 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \\ 1&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \end{bmatrix}$ **Figure 20-12—Examples of cyclic-permutation matrices with Z=8** Table F-1 displays the "matrix prototypes" of parity-check matrices for all four coding rates at block length n=648 bits. The integer i denotes the cyclic-permutation matrix P_i, as illustrated in Figure 20-12. Vacant entries of the table denote null (zero) submatrices. Table F-2 displays the matrix prototypes of parity-check matrices for block length n=1296 bits, in the same fashion. Table F-3 displays the matrix prototypes of parity-check matrices for block length n=1944 bits, in the same fashion. 802.11 (2012)

Claim 17	Identification
	 **Figure 20-11—Puncturing at rate 5/6** 802.11 (2012)